Implementation of SVPWM control on FPGA for three phase MATRIX CONVERTER

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***Abstract*—This paper presents a simple approach for implementation of a Space Vector Pulse Width Modulation (SVPWM) Technique for control of three phase Matrix Converter (MC) using MATLAB/Simulink & FPGA Software. The Matrix converter is a direct AC/AC Power conversion without an intermediate DC link. This converter is inherently capable of bi-directional power flow and also offers virtually sinusoidal input currents. The SVPWM technique improves good voltage transfer ratio with less harmonic distortion. This paper presents FPGA test bench waveforms & MATLAB simulations of SVPWM pulses and output waveforms for three phase matrix converter.**

Index Terms—Matrix Converter, Space Vector Modulation, FPGA.

I. INTRODUCTION

In recent two decades, there is an observed need to increase the quality and the efficiency of the power supply and the power usage. Three phase matrix converter becomes a modern energy converter and has emerged from the previously conventional energy conversion modules. It fulfils all requirements of the conventionally used rectifier-dc link- inverter structures. Some advantages of the matrix converter are: use of direct AC-AC poly phase power conversion, inherent bidirectional power flow capability, input/output sinusoidal waveforms with variable output voltage amplitude and frequency, input power factor control despite the load in the output side and a simple, compact power circuit because of the elimination of bulky reactive elements. MC has some limitations too. The most important is the voltage transfer ratio limitation, with a maximum value of 0.86 and Lack of required Bidirectional switches. The direct connection between input and output causes a great sensibility to grid distortions [1]. Fig. 1 shows three-phase AC-to-AC matrix converter with nine bi-directional switches connected in a matrix form. The switching constraints are (i) input phase can never be short circuited as the converter is supplied by voltage sources (ii) the output phases must not be left open, due to the inductive nature of the load. The input LC filter eliminates high frequency ripples in the input current and restricts the rise in voltage due to switching off the input line current. The switches can connect any input phase to any output phase at any instant and hence it is possible to synthesize the output voltages from input voltages and input currents from the output currents using a suitable modulation method (e.g. [2], [3], [4], [5]).

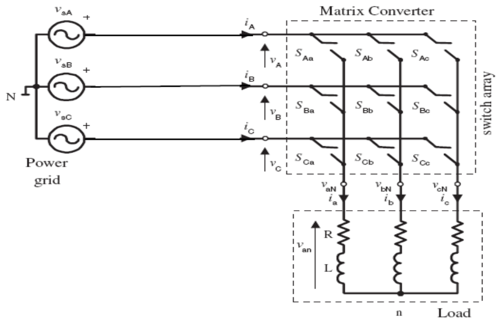

Fig 1 Three phase ac to ac matrix converter with bidirectional switches and inductive load

Presently FPGA's are replacing DSP's in many applications due to some advantages. Multiple operations can be executed in parallel so that algorithm can run much faster which is required by the control system. The available simulation software for electronic circuits or dynamic circuits can be classified into two main categories: Programming and Block Designing. In this work a VHDL coding was written for each block and simulated in Xilinx Simulator. In this paper the application of FPGA to the indirect Space Vector PWM technique of Matrix converter is described and the test bench wave forms of each block are presented.

II. SPACE VECTOR MODULATION

The mostly used modulation method for matrix converter is the space vector Pulse Width modulation (SVPWM). The matrix converter is modelled as two stage back–to–back converters, a rectification stage to produce constant imaginary DC link voltage per switching period and an inverter stage to provide the three phase output voltage. There is fictitious DC bus without any DC energy storage component between the rectification and inversion. Using this connection,

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matrix converter can be controlled as well as conventional SVM (e.g. [6], [7]). In order to obtain sinusoidal input and output currents, the SVM is carried out in terms of voltage source rectifier (VSR) input phase currents and voltage source inverter (VSI) output line voltages, which is illustrated in Fig. 2 and Fig. 3 and duty cycles are calculated as follows.

A. Rectifying Stage Modulation

The expression of input currents can be found in terms of switching state and DC link for rectifier side is given in (1)

iaibic = SpaSpbSpcSnaSnbSnc I dc+I dc- (1)

An "ON" state of a switch is denoted by "1" and the "OFF" state is denoted as "0". The input phases can never be shorted; hence the allowable switching states for rectifier side are shown in Fig. 2. Now applying the three-phase to spatial (two-axis) co-ordinate transform to the allowable switch states, the vectors obtained are of constant magnitude and phase are given in (2)

$$I_i = 2/3(i_a + i_b\, e^{j2\pi/3} + i_c\, e^{j4\pi/3}) \quad (2)$$

Hence these vectors are called the switching state vectors (SSVs). These SSVs are plotted in Fig. 2 and the space vector hexagon is shown. At any instant the desired input rotating current vector $I_i = I_{im}\, e^{j(\omega_i t - \varphi_i)}$ can be approximated by two adjacent switching state vectors and zero switching state vector as $I_i = I_\mu + I_\gamma + I_o$ .Fig. 2 shows the input current hexagon with six sectors formed by switching state vectors and the approximation of I_i .

From trigonometry,

$$I_\gamma = |\, I_i\, |\sin(60^0 - \theta_{sc}) / \sin 60^0 \quad (3)$$

$$I_\mu = |\, I_i\, |\sin(\theta_{sc}) / \sin 60^0 \quad (4)$$

But, $I_1.T_\gamma / T_s = I_\gamma$ (5)

$$I_2.T_\mu / T_s = I_\mu \quad (6)$$

If the duty cycle (d_γ) is defined as

$$d_\gamma = T_\gamma / T_s \quad (7)$$

Then, $d_\gamma = m_c.\ \mathrm{Sin}\,(60^0 - \theta_{sc})$ (8)

Similarly,

$$d_\mu = T_\mu / T_s = m_c.\ \mathrm{Sin}\,(\theta_{sc}) \quad (9)$$

And Zero Timing:

$$d_{0c} = T_{0c} / T_s = 1 - d_\mu - d_\gamma \quad (10)$$

Where, $0 \le m_c = I_{im} / I_{DC} \le 1$ (11)

and (T_s) is the total sampling time period or switching time.

So, $I_i = I_1.d_\gamma + I_2.d_\mu + I_0.d_{0c}$ (12)

The left –alignment of gate pulses for rectifier side becomes d_γ ▪ d_μ ▪ d_{0c}

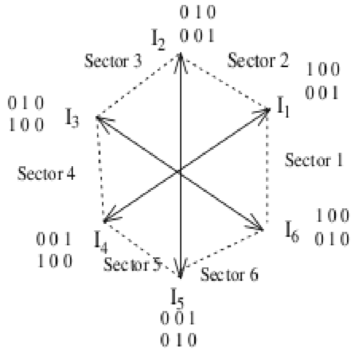

Figure 2. Input current hexagon and approximation of input rotating current vector

B. Inverting Stage Modulation

Similarly the expression of output voltages in terms of switch states and input DC link voltage for VSI side is given as in (13)

v Anv Bnv Cn = SApSAnSBpSBnSCpSCn +V dc-V dc (13)

The output phases of MC should not be open circuit. The allowable switching matrices for VSI side are shown in Fig. 3. Equation (14) indicates three –phase to spatial (two axis) co-ordinate transform as VSR side,

$$V_o = 2/3(V_{AB} + V_{BC}\, e^{j2\pi/3} + V_{CA}\, e^{j4\pi/3}) \quad (14)$$

The resulting switching state vectors are obtained and the VSI hexagon is formed. The desired output rotating voltage vector, is approximated by two adjacent switching state vectors and zero switching state vector at any instantas shown in (15).

$$V_o = 3\, V_{om}\, e^{j(\omega o t - \varphi o + \pi/6)} \quad (15)$$

Fig. 3 shows the VSI hexagon with six sectors and of V_o as, $V_o = V_\alpha + V_\beta + V_o$ at any instant

$$V_\alpha = |V_o|\, \sin(60^0 - \theta_{sv}) / \sin 60^0 \quad (16)$$

$$V_\beta = |V_o| \sin(\theta_{sv}) / \sin 60^0 \quad (17)$$

But, $V1.T_\alpha / T_s = V_\alpha$ (18)

And, $V2.T\beta / T_s = V_\beta$ (19)

Hence, $d_\alpha = T_\alpha / T_s = m_v.\ \mathrm{Sin}\,(60^0 - \theta_{sv})$ (20)

$$d_\beta = T_\beta / T_s = m_v.\ \mathrm{Sin}\,(\theta_{sv}) \quad (21)$$

and, $d_{0v} = T_{0v} / T_s = 1 - d_\alpha - d_\beta$ (22)

where, $0 \le m_v = (3\ V_{om}) / V_{DC} \le 1$

And T_s is the total sampling or switching time

So, $V_o = V_1.d_\alpha + V_2.\ d_\beta + V_o.\ d_{ov}$ (23)

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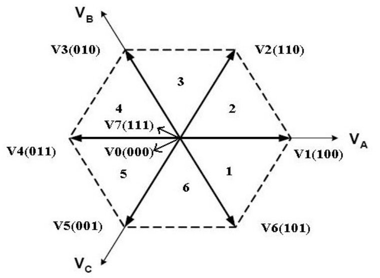

Figure 3. Output voltage Hexagon and the decomposition of output rotating voltage vector

The left –alignment of gate pulses for rectifier side becomes

$$d_\alpha \;▪\; d_\beta \;▪\; d_{0v}$$

C. Entire Matrix Converter Modulation

Now combining both the VSR and VSI modulation strategies, the switching pattern for converter is generated.

The five step left–alignment of gate pulses are formed.

dαγ ▪ dβγ ▪ dαμ ▪ dβμ ▪ do [3].

$d_{\alpha\gamma} = d_\alpha \,.\, d_\gamma = m.\ \sin(60^0 - \theta_{sv}).\ \text{Sin}\ (60^0 - \theta_c) = T_{\alpha\gamma} / T_s$

$d_{\beta\gamma} = d_\beta .\ d_\gamma = m.\ \sin(\theta_v).\ \text{Sin}\ (60^0 - \theta_{sc}) = T_{\beta\gamma} / T_s$

$d_{\alpha\mu} = d_\alpha .\ d_\mu = m.\ \sin(60^0 - \theta_v).\ \text{Sin}\ (\theta_{sc}) = T_{\alpha\mu} / T_s$

$d_{\beta\mu} = d_\beta .\ d_\mu = m.\ \sin(\theta_{sv}).\ \text{Sin}\ (\theta_c) = T_{\beta\mu} / T_s$

$d_o = 1 - d_{\alpha\gamma} - d_{\beta\gamma} - d_{\alpha\mu} - d_{\beta\mu} = T_o/T_s$

Since both the VSR and the VSI hexagons contain six sectors, there will be 36 operating sectors. For each sector the switching pattern for nine-switch matrix converter is obtained from the location of input current and output voltage rotating vectors. For this particular case during dβγ duration, I2 is active at rectifier side and V6 is active at inverter side. From switching status of both VSR and VSI part it can be seen that the input phase 'a' is connected with output phase 'A' & 'C', input phase 'c' is connected with output phase 'B', hence for nine-switch matrix converter S_{aA}, S_{cB}, S_{aC} are 'ON' [8], [9]. Similarly for dαγ duration S_{aA}, S_{cB} and S_{cC} are ON. For input phase 'a' is connected with output phase 'A', input phase 'c' is connected with output phase 'B' & 'C' Sector (V1–I2).

III. FPGA IMPLEMENTATION OF SVPWM

The SVPWM method for control of the nine-switch matrix converter contains the following steps:

1. Generation of sampling interrupts from FPGA clock 50MHz.
2. Generation of address for pulse width data.
3. Loading pulse width data on a data bus in ROM
4. Calculation of duty cycles at each sampling interval in Pulse width Timer block.
5. Generation of 9 switching pulses by using pulse width data in firing pulse block.
6. Distribution of switching pulses to nine-switch matrix converter.

Quantizer 100 Hz (voltage Sector (RYV, YBV, BRV)) & 600Hz (current sector (RYI, YBI, BRI)) blocks will give the sector selection pulses to firing logic block. These block pulses are synchronized with the master clock. The block diagram is shown in Fig. 4 Sampling timer is an auto reset count up timer and produces a pulse at the end of counting and begins counting from start. Sampler block will give the interrupt (INTRPT) at every sample instant. The RESET pin when HIGH causes the timer to begin up counting from 'zero' value irrespective of current value. Address counter keeps track of the address of data in memory blocks. It is incremented when it is triggered at its INTRPT pin by a pulse. It continuously outputs the address value whenever it is incremented, it sends out a pulse at the ADDR_OUT pin. When the address count reaches maximum value, it is changed to zero when an interrupt comes. When the RESET pin is made HIGH, the address is made zero. ROM has a 2-Bit address bus and a 16-bit data bus. It has an Output Enable (OE) pin which has to be made HIGH in order to read data from the location specified by address on address lines. Whenever the OE pin is made HIGH, the data is output on the data bus and a pulse is output on the DATA_OUT pin. Pulse width timer is employed to produce firing pulses for the gates of the MOSFETs in the converter. This is a simple countdown timer that takes 16-bit count values and down counts to zero and stops. In order to load the count value and begin the counting, a pulse is required at the START pin of the timer. While counting, the timer sends a HIGH at the PULSE pin. When the counting is finished, the PULSE pin is made LOW and a pulse is sent at the PULSE_END pin. This block essentially consists of demuxes and depending on the functions given, gives the appropriate pulse to each device. There are six controlling inputs RYV, YBV, BRV, RYI, YBI, BRI that decide which output pin is to remain HIGH.

The quantizer blocks generate RY, YB and BR signals that are used to determine the sector of the voltage & current space vector as shown in Table I. The pulses produced at every 60^0,when a sector begins, are fed to the RESET pins of Sampling Timer and the Address Counter. So, the circuit is synchronized with the supply at the start of every sector. In a sector, the sampling timer produces pulses after every sampling period. These pulses are fed to the INTRPT pin of the Address Counter thereby updating the address.

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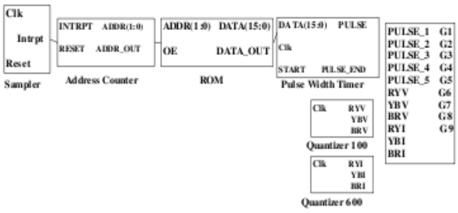


Figure 4. Designed Blocks in XILINX FPGA implementation

The VHDL coding was written for each block [10], [11]. The next logical step is synthesis of the design. Xilinx ISE 10.1 synthesis tool is used for the synthesis. Next implement design step is executed. Before this step the location constraints are assigned in the .ucf file. The translation step takes the .ngr file obtained during synthesis as one of its input. This results in formation of .ngd file through NGDBUILD process. Then mapping is carried out followed by place and route. Finally the .bit file generated is ready to be downloaded in to the FPGA. FPGA is configured using USB cable and program is stored in the on-board SRAM. Thus FPGA functions as the firing pulse generation circuit for the power module. The pulses generated are in accordance with the SVPWM Scheme. The value of modulation index m has been taken constant and all firing pulses durations have been calculated using this value [8].

System design parameters

1. Sampling Frequency = 7200 Hz
2. Master clock frequency = 50MHz
3. Modulation Index (m) = 0.75

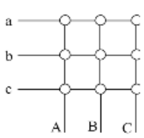
The logic circuit inside decoder generates SVPWM pattern gives below with proper switching sequence.

$$d_{\alpha\gamma} \blacksquare d_{\beta\gamma} \blacksquare d_{\alpha\mu} \blacksquare d_{\beta\mu} \blacksquare d_o$$

The switching sequence for operation of SVPWM of Matrix converter is tabulated in Table 1for an output frequency of 100Hz. The numbering of switches in the matrix converter are shown in Fig. 5. The switches are in a Matrix form in Fig. 5a and the switch numbering is shown in Fig. 5b.

Selected Device is xc3s500e-4fg320

Input Lines: a, b, c, Output Lines: A,B,C



Switch	No	Switch	No
aA	1	cB	6
bA	2	aC	7
cA	3	bC	8
aB	4	cC	9
bB	5		

Fig 5 (a) Switches in Matrix Form (b) Switch Numbering

IV. EXPERIMENTAL RESULTS

The Xilinx simulation result of each pulse generation block has been shown and MATLAB/Simulink of matrix converter results is also shown. The behavioural simulation was used in the Xilinx ISE 10.1 simulator. The system Designed for 50MHz clock. The simulation clock value was set to time period of 20ns and duty cycle of 50%. It can also be noted that each building block can be individually simulated to observe its behaviour.

The Test bench waveforms of each block in Fig. 6

A Sampling Block:

The input to this block is 50MHz clock. The output is an interrupt signal gives at every 138.8µs as shown in Fig. 6(a).

B Address Counter:

Whenever the interrupt comes it increments the address of pulse data and after reaching maximum address value it starts from initial value as shown in Fig. 6(b).

C Read only Memory:

When OE pulse comes the 16-bit data loads on DATA BUS depend on the address in the address bus as shown in Fig. 6(c).

D Pulse Width Timer:

Whenever the START pulse comes the PULSE has started. Pulse width depends on the data in DATABUS. At the end of pulse small PULSE_END signal is generating as shown in Fig. 6(d).

E Firing Logic Block:

This block generates switching pulses according to the pulse width timer pulses and quantizer pulses.

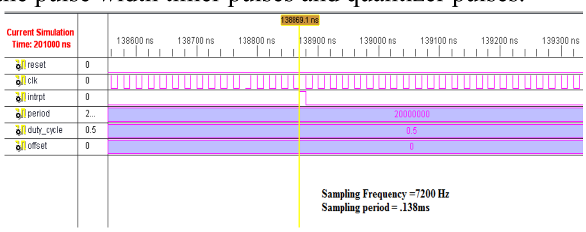


Fig 6 (a) Interrupt signal from Sampling Block

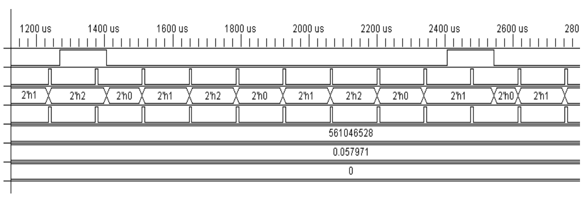


Fig 6 (b) Loading Address on address Bus in Address counter

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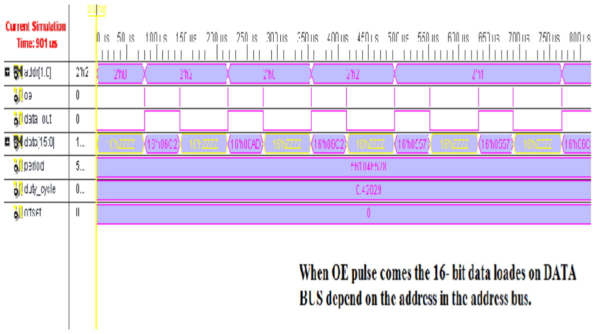

Figure 6. (c) Loading Data on data Bus in ROM

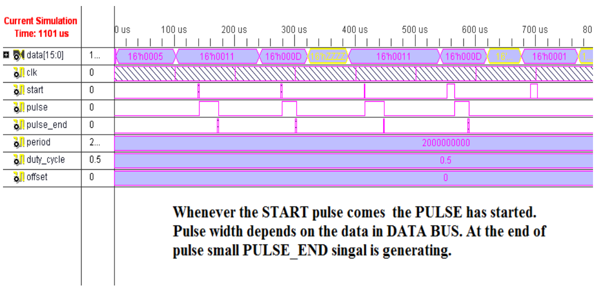

Figure 6. (d) Pulses from Pulse Width Timer

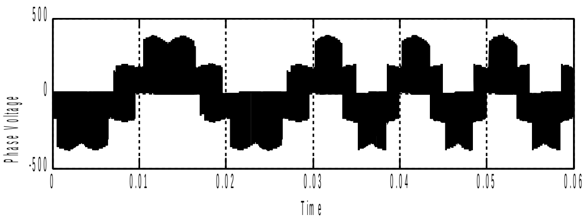

Figure 7. (a) Phase Voltage with 50Hz (0- 0.03 sec), 100Hz (0.03-0.06) sec

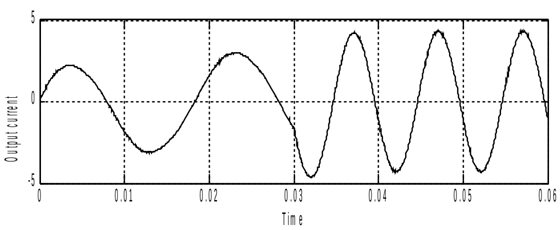

Figure 7. (b) Output current with 50Hz (0-0.03 sec), 100Hz (0.03-0.06) sec

The output phase voltage and current with 50Hz and 100Hz frequencies are shown in Fig. 7(a) & Fig. 7(b). Line voltage with 50Hz and 100Hz shown in Fig. 7(c). Output RMS Voltage changes as modulation index is changed (0.3 & 0.5) shown in Fig. 7(c).

TABLE I
SWITCHING TABLE

RYV	YBV	BRV	RYI	YBI	BRI	Sector No V,I	αγ	βγ	αμ	βμ	00
1	0	1	1	0	1	1,1	1,	1,	1,	1,	1,
0	1	0	0	1	0	4,4	5,7	5,8	6,7	6,9	4, 7
1	0	1	1	0	0	1,2	1,6	1,6	2,6	2,6	1,
0	1	0	0	1	1	4,5	7	9	8	9	47
1	0	1	1	1	0	1,3	2,6	2,6	2,4	2,4	2,
0	1	0	0	0	1	4,6	8	9	8	7	58
1	0	1	0	1	0	1,4	2,4	2,4	3,4	3,4	2,
0	1	0	1	0	1	4,1	8	7	9	7	58
1	0	1	0	1	1	1,5	3,4	3,4	3,5	3,5	3,
0	1	0	1	0	0	4,2	9	7	9	8	69
1	0	1	0	0	1	1,6	3,5	3,5	1,5	1,5	3,
0	1	0	1	1	0	4,3	9	8	7	8	69
1	0	0	1	0	1	2,1	1,5	1,4	1,6	1,4	2,
0	1	1	0	1	0	5,4	8	8	9	9	58
1	0	0	1	0	0	2,2	1,6	1,4	2,6	2,5	3,
0	1	1	0	1	1	5,5	,9	,9	,9	,9	69
1	0	0	1	1	0	2,3	2,6	2,5	2,4	2,5	3,
0	1	1	0	0	1	5,6	,9	,9	,7	,7	69
1	0	0	0	1	0	2,4	2,4	2,5	3,4	3,6	1,
0	1	1	1	0	1	5,1	,7	,7	,7	,7	47
1	0	0	0	1	1	2,5	3,4	3,6	3,5	3,6	1,
0	1	1	1	0	0	5,2	,7	,7	,8	,8	47
1	0	0	0	0	1	2,6	3,5	3,6	1,5	1,4	2,
0	1	1	1	1	0	5,3	,8	,8	,8	,8	58
1	1	0	1	0	1	3,1	1,4	2,4	1,4	3,4	1,
0	0	1	0	1	0	6,4	,8	,8	,9	,9	47
1	1	0	1	0	0	3,2	1,4	3,4	2,5	3,5	1,
0	0	1	0	1	1	6,5	,9	,9	,9	,9	47
1	1	0	1	1	0	3,3	2,5	3,5	2,5	1,5	2,
0	0	1	0	0	1	6,6	,9	,9	,7	,7	58
1	1	0	0	1	0	3,4	2,5	1,5	3,6	1,6	2,
0	0	1	1	0	1	6,1	,7	,7	,7	,7	58
1	1	0	0	1	1	3,5	3,6	1,6	3,6	2,6	3,
0	0	1	1	0	0	6,2	,7	,7	,8	,8	69
1	1	0	0	0	1	3,6	3,6	2,6	1,4	2,4	3,
0	0	1	1	1	0	6,3	,8	,8	,8	,8	69

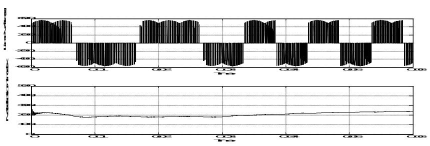

Figure 7. (c) Line Voltage with 50Hz (0 - 0.03 sec), 100Hz (0.03 - 0.06) sec and Modulation Index is 0.3 (0 - 0.03 sec), 0.5 (0.03 - 0.06) sec

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V. CONCLUSION

The versality and reconfigurability of FPGA gives a lot of options in the hands of user. The user can modify the VHDL code and made the FPGA function as per his requirements. In the current mode modulation index has been kept constant; the code can be modified to incorporate the on-line calculation of modulation index. However the program developed for this must support floating point operations. In this paper implementation of Space Vector Pulse Width Modulation by using FPGA has been shown. The MATLAB simulation results of SVPWM MC Output and SVPWM signals have been shown. The sampling frequency is 7200Hz hence closed loop control can be programmed for drive application. The FPGA signals can be directly interfaced to hardware. Yet all the advantages of the digital structure, i.e. high flexibility, parameterization capability, etc. Remain unchanged. Furthermore, FPGA is hardware realization of a digital data processing algorithm, hence the reliability of the control system is improved.

REFERENCES

[1] J. Vadillo, J.M. Echeverría, L. Fontán, M. Martínez-Iturralde and I. Elósegui, "Modelling and Simulation of a Direct Space Vector Modulated Matrix Converter using different Switching Strategies" SPEEDAM 2008, International Symposium on Power Electronics, pp. 944-949.

[2] S. Mukherjee, A. Dasgupta, M. Sengupta, P. Syam and A. K. Chattopadhyay, "Implementation of indirect SVPWM control for a three phase matrix converter using TMS32OLF24O7A in combination with FPGA EPIC6Q24OC8" proc of IEEE, pp.1442-1447.

[3] H. Hotate and K. Matsuse "Basic characteristics of Matrix – converter controlled by space vector modulation considering input voltage conditions" proc of conf, pp.719-723.

[4] J. Rodriguez, "A new control technique for ac-ac converters," in *Proc. IFAC Control in Power Electronics and Electrical Drives 1983,* pp.*203*-208.

[5] A. Ishiguro, K. Inagaki, M. Ishida, **S.** Okuma, Y. Uchikawa, and K. Iwata, "A new method of PWM control for forced commutated cycloconverters using microprocessors," in *Conf Rec. IEEE Ind. Appln. Soc. Ann. Meeting,* 1988, pp.712-721.

[6] P. Wheeler, J. Rodriguez, J. Clare, L. Empringham and A. Weinstein, "Matrix Converters: A technology review", *IEEE Transactions on industrial Electronics,* 49, pp. 276-288, April 2002.

[7] L. Huber and D. BorojeviC, "Space vector modulation with unity input power factor for forced commutated cycloconverters," in *Conf Rec .IEEE Ind. Applicat. Soc. Annu. Meeting,* 1991, Part I, pp. 1032-1041.

[8] H.J. Cha and P.N. Enjeti, "Matrix converter –fed ASDs", Industrial Application Magazine, IEEE, Vol 10, Issue 4, July -Aug 2004, pp.33-39.

[9] A. Alesina and M. Venturini, "Analysis and design of optimumamplitude nine-switch direct ac-ac converters," *IEEE Trans. Power Electron.,* vol. 4, No. 1**,** pp.101-112, Jan. 1989.

[10] J. Bhasker, "A VHDL Primer," ISBN 978-81-7758-200-0, Third Edition, Pearson Education.

[11] Xilinx ISE 10.1 user Guide, www.xilinx.com

DOI: 01.ijcom.01.02.06